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Low Latency Ifft Design for Ofdm Systems

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Abstract : *OFDM is a multi carrier modulation technique used in the various digital communication systems like 3G GSM, WiMAX, and LTE etc. The main advantage of this transmission technique is their hardiness to channel fading in wireless communication environment. Extensive connectivity, low latency and very high data transfer are the unique features of 5G networks. The digital audio Broadcasting, asynchronous digital subscriber line (ADSL) and high bit-rate digital subscriber line (HDSL) systems etc are some of the applications of OFDM in communication. Fast Fourier transform (FFT) and Inverse Fast Fourier Transform (IFFT) are two digital signal processing algorithm involved in OFDM system which are efficient for long instances in digital communication. The core processing block in an OFDM transmitter is the Inverse Fast Fourier Transform. For long instances, Single-Path Delay-Feedback (SDF) FFT architectures minimize required memory, which can dominate circuit area and power dissipation. The 8-point IFFT with radix-2 Single Delay Feedback algorithm have been analyzed for N=256 samples and incorporated in the design.*

Keywords - *3G GSM, WiMAX, LTE, ADSL, HDSL, Radix-2*

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I. Introduction

Low latency Inverse Fast Fourier Transform (IFFT) is one of the design methods for OFDM systems which support full-duplex Frequency Division Duplex (FDD). To support full-duplex FDD OFDM systems means that transmission and reception are simultaneously performed. In order to reduce the IFFT output latency, we propose the reordering scheme of IFFT input data. By using the reordered IFFT input data, both the output latency and the memory size in the first stage of IFFT are significantly reduced. In this case, the FFT/IFFT processing can't be shared with one FFT/IFFT processor and therefore, they must be designed separately from each other. In the multi carrier systems like OFDM, IFFT/FFT is one of the key blocks in the physical layer implementation, since IFFT/FFT blocks require large amount of area, processing latency and power consumption. SDF approach based on radix-2 algorithm is frequently used for its low cost and high efficiency.

II. Description

2.1. OFDM SYSTEMS

Orthogonal Frequency Division Multiplexing (OFDM) is adopted as standard in the many wireless communication applications since OFDM has the good performances of the systems under multipath fading channel. OFDM Signal transmission and reception using IFFT and FFT block is shown in figure1. In the OFDM systems, input data of the IFFT corresponding to guard band are assigned as null.

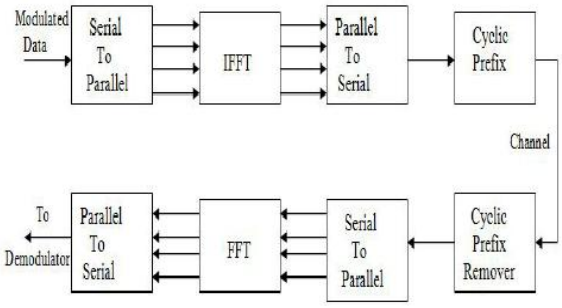

Fig.1: OFDM Signal transmission and reception using IFFT and FFT block

2.2. IFFT

Low latency IFFT design method is proposed based on the fact that there are many null as an input data of IFFT. The common way to implement the inverse Fourier transform is by an IFFT algorithm. The equation (1) is the basic equation to calculate FFT.

$$X(k)=\sum_{n=1}^{N-1} x(n)e^{-j2\pi kn/N} \quad ,k=0,\ldots,N-1 \rightarrow (1)$$

On the other hand, the equation (2) is used to calculate IFFT.

$$x(n)=\frac{1}{N}\sum_{n=1}^{N-1} X(k)e^{-j2\pi kn/N} \quad ,n=0,\ldots,N-1 \rightarrow (2)$$

Where N is the transform size or the number of sample points in the data frame, X (k) is the frequency output of the FFT at k- th point where k=0, 1… N-1 and x (n) is the time sample at nth point with n=0, 1… N-1[1]. IFFT is a fast algorithm for IDFT operation. The twiddle factor (TW) W^i means the e^j2πk/N. The data flow for 8-point radix2 IFFT is shown in figure 2. In conventional radix-2 based SDF IFFT architecture, for the even cycles of $N/2^i$ clock, input signals of *i*-th stage are bypassed at butterfly block and stored at the memory in each stage. For the odd cycles of $N/2^i$ clock, butterfly operation compute at the same time and the addition outputs of butterfly are sent to next stage while the subtraction outputs of butterfly are stored at the memory in current stage.

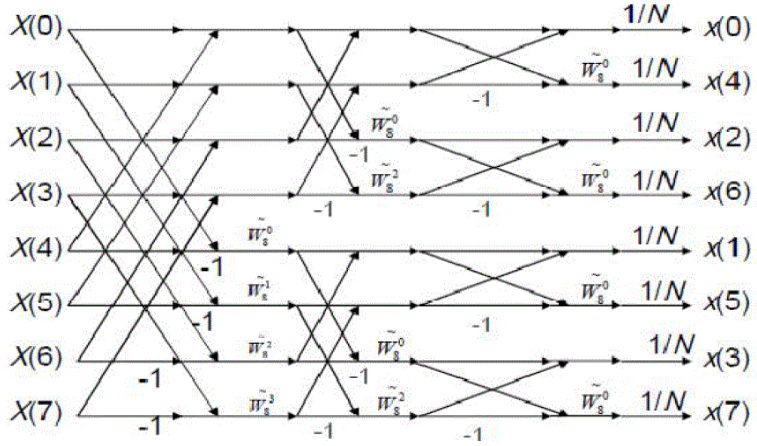

Fig.2: Data flow for 8-point radix2 IFFT

2.3. RADIX-2

Radix-2 IFFT algorithm is used to reduce the order of computational complexity by decimating even and odd indices of input samples. IFFT architectures are mainly classified in two ways: Memory based architecture and pipelined based architecture. Popular pipelined architectures are based on radix-2 or radix-4 algorithms. Higher the radix, lower the computational complexity. Tradeoff for the selection of architecture is the requirement of length of IFFT for the particular application. Here Radix-2 Single Delay Feedback path is used. These provide memory feedback path to manage some butterfly outputs during each stage. This is one of the architecture for implementing IFFT on FPGA for multiple output orthogonal frequency division multiplexing. Radix-2 Single-path Delay Feedback [2] uses the registers more efficiently by storing the butterfly output in feedback shift registers. A single data stream goes through the multiplier at every stage. It has same number of butterfly units and multipliers as in R2MDC approach, but with much reduced memory requirement N-1registers. Its memory requirement is minimal. Where first N/2 input samples are stored in FIFO and operation starts when N/2+1st data is available at the input to the butterfly unit [3]. For designing N-stage pipelined FFT/IFFT architecture same SDF module is repeated for $\log_2 N$ time. It gives flexibility in design of any point FFT/IFFT. SFG shown in fig. 2 can be implemented using R2SDF. Block diagram for the same is shown in figure 3.

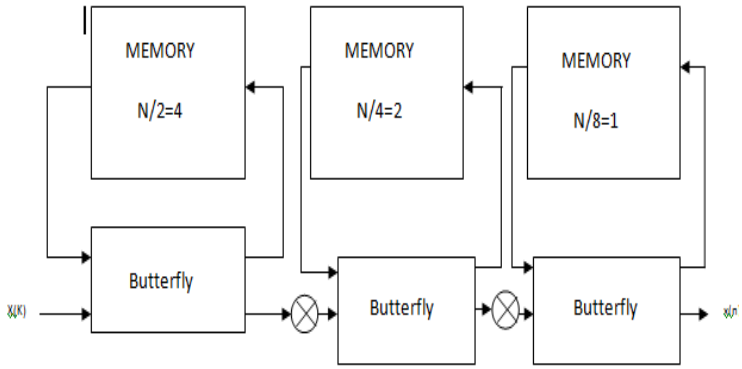

Fig.3: Structure of 8-point radix2 IFFT

Figure 4 represents the RTL view of an 8 point IFFT.

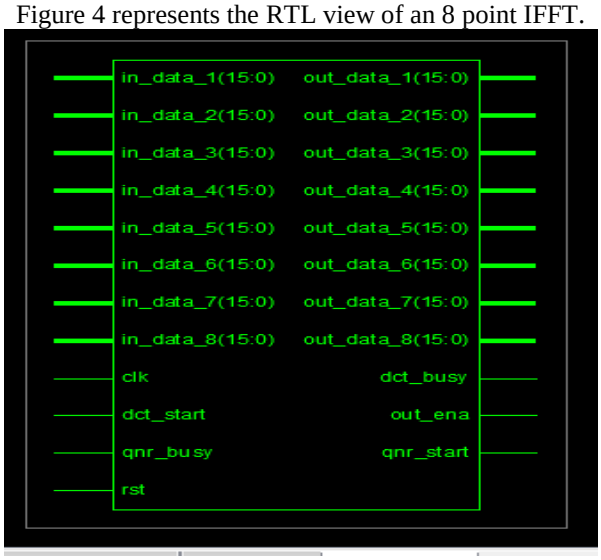

Fig.4: RTL view of an 8 point IFFT

2.4. POWER RESULT

The power result shows the overall power performance of 8 point IFFT algorithm. The figure 5 shows the leakage power result for 8-IFFT algorithm. Layout generated using cadence is shown in figure 6.

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
dct2d	8392	323045.492	33402952.486	33725997.978

Report Power

Generated by: Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1 (Aug 11 2015)
Generated on: Jun 12 2018 17:07:46
Module: dct2d
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
dct2d	8392	323045.49	29081189.59	4321762.89	33402952.49

Fig.5: Analysis of power for 8 point IFFT in Xilinx and cadence

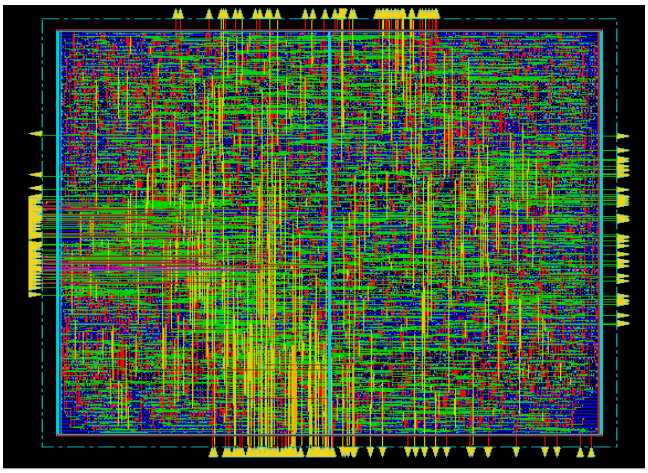

Fig.6: Layout of 8 point IFFT generated using cadence

III. Conclusion

The 8-point Radix-2 IFFT is designed for OFDM system and the power result and timing is analyzed in Xilinx and Cadence.

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